WHAT IS CLAIMED IS:

1. A memory device comprising:

an interface which interfaces with an external device;

an IC chip which stores one or more application programs and executes said application programs;

a memory which stores associated data associated with said one or more application programs; and

a controller connected with said interface, said IC chip, and said memory;

wherein said controller, in response to a predetermined command received from said external device by way of said interface, performs transfer of said associated data between said IC chip and said memory without passing said associated data to said host device during transfer of said associated data between said IC chip and said memory.

2. A memory device as recited in claim 1 wherein:

said memory is divided into a plurality of blocks; and

each of said plurality of blocks to be assigned to an application program to store said associated data associated with said assigned application program.

3. A memory device as recited in claim 2 wherein said memory includes a management area to store an association between an application ID used to identify each one of said application programs and an operation code used to transfer said associated data associated with said one application program between said memory and said IC chip.

4. A memory device as recited in claim 3 wherein said memory is controllable to operate in a locked mode to disable changing and adding and deleting an application ID in said memory associated with an application program stored in said IC chip when at least one application program is stored in said IC chip, and an unlocked mode to permit changing and adding and deleting an application ID in said memory.

5. A memory device as recited in claim 3 wherein said controller compares an application ID from said IC chip with an application ID from said memory, and, if there is a match between said application ID from said IC chip and said application ID from said memory, allows transfer of said associated data associated with said application program identified by said application ID between said IC chip and said memory.

6. A memory device as recited in claim 3 wherein said operation code is unique to said application ID associated with said operation code.

7. A memory device as recited in claim 1 wherein said associated data is already stored in said memory when said memory device is first used.

8. A memory device as recited in claim 1 wherein said controller which performs transfer of associated data associated with an application program between said IC chip and said memory, in response to said predetermined command, by a transfer command associated with said application program sent from said memory to said IC chip.

9. A memory device comprising:

an IC chip which executes one or more application programs;

a memory divided into a plurality of blocks, each block to be assigned to an application program executed by said IC chip; and

a controller controlling access to said memory and said IC chip;

wherein said memory stores one or more command codes used to allow said controller to query said IC chip regarding an instruction to perform an operation, said instruction being issued by said IC chip to said controller, each command code being associated with an application ID for identifying an application program;

wherein, in response to an application ID associated with an application program, said application ID being sent by said IC chip to said controller for executing said application program, said controller identifies, out of said one or more command codes stored in said memory, a command code associated with said application ID from said IC chip, and sends said identified command code to said IC chip; and

wherein, in response to an instruction to perform an operation issued by said IC chip to said controller based on said identified command code, said controller performs said operation.

10. A memory device as recited in claim 9 wherein said command code includes a first transfer command for transferring data to be written to a block in said memory from said IC chip to said controller and a second transfer command for transferring data read from a block in said memory by said controller to said IC chip.

11. A memory device as recited in claim 10 wherein said IC chip sends the application ID to said controller for executing said application program based on a request from the controller in response to an external command received by the controller, and wherein the external command differs from the first transfer command and the second transfer command of the command code.

12. A memory device as recited in claim 10 wherein the instruction to perform an operation issued by said IC chip specifies which of the first transfer command and the second transfer command is to be performed.

13. A memory device comprising:

an IC chip which executes one or more application programs;

a memory divided into a plurality of blocks, each block to be assigned to an application program executed by said IC chip; and

a controller controlling access to said memory and said IC chip;

wherein said controller, in response to a first command from an external device, assigns a usage privilege for a block in said memory to a particular application program to be executed by said IC chip; and, in response to a second command from the external device, changes from an unlocked state allowing execution of an operation in response to said first command to a locked state disallowing execution of said operation in response to said first command.

14. A memory device as recited in claim 13 wherein:

said memory stores management information used to manage associations between identifiers for said blocks and identifiers for application programs for which usage privilege has been assigned for said blocks;

said controller allows contents of said management information to be changed in said unlocked state; and

said controller disallows contents of said management information to be changed in said locked state.

15. A memory device as recited in claim 13 wherein:

said memory stores management information used to manage associations between identifiers for said blocks and identifiers for application programs for which usage privilege has been assigned for said blocks; and

said controller, when said usage privilege for a block is assigned to an application program, adds an identifier for said application program associated with an identifier for said block to said management information.

16. A memory device as recited in claim 13 wherein:

said memory stores a flag for identifying whether execution of said operation in response to said first command is allowed or disallowed; and

said controller changes said flag when changing from said unlocked state to said locked state in response to said second command.

17. A memory device as recited in claim 13 wherein said controller changes from said locked state to said unlocked state in response to a third command from said external device.

18. A memory device as recited in claim 17 wherein:

said memory stores a reference password; and

said controller changes from said locked state to said unlocked state in response to said third command if a password received from said external device matches said reference password in said memory.

19. A memory device as recited in claim 13 wherein said controller disables usage privilege for a block assigned for an application program in response to a fourth command from said external device.

20. A memory device as recited in claim 19 wherein:

said memory stores management information used to manage associations between identifiers for said blocks and identifiers for application programs for which usage privilege has been assigned for said blocks; and

said controller removes from said management information an identifier for said application program associated with an identifier for said block when disabling usage privilege for said block assigned for said application program.

21. A memory device as recited in claim 13 wherein said memory includes a first area for storing data received from said external device and a second area comprising said blocks for which usage privilege is assigned for said application programs.

22. A memory device as recited in claim 21 wherein said controller generates, for each application program, transfer command codes for identifying transfer commands for receiving data to be written to said second area of said memory from said IC chip and for sending data to be written to said second area to said IC chip.

23. A memory device as recited in claim 22 wherein said transfer command codes are unique to each application program.

24. A memory device comprising an interface which interfaces with an external device and a memory which includes at least seven terminals, wherein said interface is configured to perform the following:

receiving a lock command from said external device, said lock command setting said memory to a locked state;

receiving a read command from said external device to read from said memory; and

sending a response rejecting said read command to said external device when said memory is in said locked state.

25. A memory device as recited in claim 24 wherein said interface is configured to perform the following:

receiving an unlock command from said external device, said unlock command setting said memory to an unlocked state;

receiving a read command from said external device to read from said memory; and

sending data read from said memory to said external device when said memory is in said unlocked state.

26. A memory device as recited in claim 25 wherein receiving said unlock command comprises receiving a password, said unlock command setting said memory to said unlocked state if said received password matches a reference password stored in said memory.

27. A memory device as recited in claim 26 wherein said reference password is set up based on the lock command setting said memory to said locked state.

28. A memory device as recited in claim 25 wherein said data sent to said external device comprises output data in an output data field including a first control byte, a second control byte, and trailing output data.

29. A memory device as recited in claim 28 wherein said data sent to said external device further comprises at least one status word byte.

30. A memory device as recited in claim 29 wherein said data sent to said external device further comprises dummy data and a response length which is used to remove said dummy data from said output data in said output data field.

31. A memory device as recited in claim 24 wherein said memory includes nine terminals.